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10/785,099	02/25/2004	Ching-Chuan Chen	8970.0007	8802

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
2629	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/785,099	CHEN, CHING-CHUAN	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3 and 5-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3 and 5-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 2,3 and 5-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 8, 12-15 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujiwara et al. (US 5,835,170).

Regarding claim 8, Fujiwara et al. disclose a liquid crystal display device comprising:

a plurality of gate lines formed in parallel to each other (Figure 1, lines 103-106);

a plurality of source lines formed in parallel to each other and orthogonal to the gate lines (Figure 1, lines 101-102); and

an array of cells formed in rows and columns, each of the cells disposed near an intersection of an N-th gate line and an M-th source line (Figure 1 shows cells between the intersections of the gate lines.), N and M being integers, further comprising:

a first capacitor formed between an electrode and an (N-2)-th gate line (Figure 1 shows capacitor 111 and column 8, lines 37-50 explain the connection to the N-2 gate line.); and

a second capacitor formed between the electrode and an (N-1)-th gate line (Figure 1 shows capacitor 110 and column 8, lines 37-50 explain the connection to the N-1 gate line.).

Regarding claim 12, Fujiwara et al. disclose the device of claim 8, wherein a signal transmitted on the M-th source line includes a first voltage level and a second voltage level (Figure 3 and column 8, line 61 to column 9, line 13 explain that signals will be transmitted for display driving. As such, a voltage will be applied to the signal lines to cause display, where the signal will contain a voltage of zero and voltage for display.).

Regarding claim 13, Fujiwara et al. disclose the device of claim 12, the first capacitor being charged to a third voltage level between the first and second voltage levels after a selection period of the previous gate line (Figure 3 shows a pulse being applied to the gate line G(n-2) which will charge the capacitor 111. See also column 8, line 61 to column 9, line 13.).

Regarding claim 14, Fujiwara et al. disclose the device of claim 12, an electrical potential of the electrode being kept at a third voltage level between the first and second voltage levels after a selection period of the (N-1)-th gate line (Column 8, line 61 to column 9, line 13 and Figures 1 and 3 explain that each capacitor 110 and 111 can store half of the charge needed, i.e. third voltage the capacitor 110 is connected to the N-1 gate line such that the electrode will be maintained at the third voltage level after N-1 is selected.).

Regarding claim 15, Fujiwara et al. disclose the device of claim 12, the first capacitor being charged to the first voltage level after a selection period of the N-th gate line from a third voltage level between the first and second voltage levels (As shown by Figures 1 and 3, capacitor 111 will be charged to the level of voltage applied at the transistor 107 dependent on the signal applied to gate line 103.).

Regarding claim 22, please refer to the rejection of claim 8, and furthermore Fujiwara et al. also disclose:

providing a signal including a first voltage level and a second voltage level from the M-th source line (Figure 3 and column 8, line 61 to column 9, line 13 explain that signals will be transmitted for display driving. As such, a voltage will be applied to the signal lines to cause display, where the signal will contain a voltage of zero and voltage for display.);

selecting an (N-2)-th gate line (Figure 3 shows gate line N-2 being selected.);

charging a first capacitor of the each of the cells to a third voltage level between the first and second voltage levels after a selection period of the (N-2)-th gate line (Figure 3 shows a pulse being applied to the gate line G(n-2) which will charge the capacitor 111. See also column 8, line 61 to column 9, line 13.);

selecting an (N-1)-th gate line (Figure 3 shows gate line N-1 being selected.);

keeping an electrical potential of a terminal of the first capacitor at the third voltage level after a selection period of the (N-1)-th gate line (Column 8, line 61 to column 9, line 13 and Figures 1 and 3 explain that each capacitor 110 and 111 can store half of the charge needed, i.e. third voltage, and thus capacitor 111 will remain charged even after N-1 is selected.);

selecting an (N)-th gate line (Figure 3 shows gate line N being selected.); and

charging the first capacitor to the first voltage level after a selection period of the N-th gate line from the third voltage level (As shown by Figures 1 and 3, capacitor 111

will be charged to the level of voltage applied at the transistor 107 dependent on the signal applied to gate line 103.).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 2-3, 5-7 and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US 2004/0119673) in view of Fujiwara et al. (US 5,835,170).

Regarding claim 2, Park discloses a liquid crystal display device comprising:

a plurality of gate lines formed in parallel to each other (Figure 2, GL1, Gli-1,...GLn.);

a plurality of source lines formed in parallel to each other and orthogonal to the gate lines (Figure 2, DL1, DL2,...DLm/2.);

an array of cells formed in rows and columns, each of the cells being formed near an intersection of one of the gate lines and one of the source lines (Figure 2 shows cells 10, 12, 14 and 16 are formed at the intersection of the gate and data lines as explained in paragraph [0074].);

a first transistor of each of the cells disposed at an N-th row and M-th column, N and M being integers, driven by an (N-2)-th gate line (Figure 2 shows that TFT4 of each cell is disposed at an N-th row and M-th column and is driven by the N-2-th gate line.); and

a second transistor of the each of the cells driven by an N-th gate line (Figure 2 shows that TFT3 of each cell is driven by the N-th gate line.).

Park fails to teach wherein each of the cells further comprises a capacitor formed between an electrode and the (N-2)-th gate line.

Fujiwara et al. disclose wherein each cell formed near an intersection of one of the gate lines and one of the source lines comprises a capacitor formed between an electrode and the (N-2)-th gate line (Figure 1 shows capacitor 111 and column 8, lines 37-50 explain the connection to the N-2 gate line.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to for the display cell taught by Park to have a capacitor as taught by Martin in order to minimize leakage currents, minimize the change in a pixel

voltage caused by a parasitic capacitor and to minimize the effects of display data dependency in the liquid crystal capacitor (See Fujiwara et al., column 8, lines 22-33).

Regarding claim 3, Park and Fujiwara et al. disclose the device of claim 2. Fujiwara et al. also disclose wherein each cell formed near an intersection of one of the gate lines and one of the source lines comprises a capacitor formed between an electrode and the (N-1)-th gate line (Figure 1 shows capacitor 110 and column 8, lines 37-50 explain the connection to the N-1 gate line.).

Regarding claim 5, Park and Fujiwara et al. disclose the device of claim 3. Fujiwara et al. also disclose the first capacitor being charged to a first voltage level in response to a fist state of a signal transmitted on the (N-2)-th gate line, and being discharged to a second voltage level in response to a second state of the signal transmitted on the (N-2)-th gate line (Figure 3 shows a pulse being applied to the gate line G(n-2) which will charge the capacitor 111, and when the pulse is taken to zero, the capacitor 111 will be discharged. See also column 8, line 61 to column 9, line 13.).

Regarding claim 6, Park and Fujiwara et al. disclose the device of claim 5. Fujiwara et al. also disclose of an electrical potential at an electrode being pulled up to a third voltage level in response to a first state of a signal transmitted on the (N-1)-th gate line, and being pulled down to the second voltage level in response to a second state of the signal transmitted on the (N-1)-th gate line (Figure 3 shows a pulse being

applied to the gate line G(n-1) which will charge the capacitor 110, and when the pulse is taken to zero, the capacitor 110 will be discharged, meaning that the potential of the electrode be changed. See also column 8, line 61 to column 9, line 13.).

Regarding claim 7, Park and Fujiwara et al. disclose the device of claim 6. Fujiwara et al. also disclose the first capacitor being charged from the second voltage level to the first voltage level in response to a first state of a signal transmitted on the N-th gate line (As shown by Figures 1 and 3, capacitor 111 will be charged to the level of voltage applied at the transistor 107 dependent on the signal applied to gate line 103.).

Regarding claim 16, this claim is rejected under the same rationale as claim 2.

Regarding claim 17, this claim is rejected under the same rationale as claim 3.

Regarding claim 18, this claim is rejected under the same rationale as claim 12.

Regarding claim 19, this claim is rejected under the same rationale as claim 13.

Regarding claim 20, this claim is rejected under the same rationale as claim 14

Regarding claim 21, this claim is rejected under the same rationale as claim 15.

7. Claims 9-11 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara et al. (US 5,835,170) in view of Park (US 2004/0119673).

Regarding claim 9, Fujiwara et al. disclose the device of claim 8.

Fujiwara et al. fail to teach of the device further comprising a first transistor including a gate coupled to the (N-2)-th gate line, and a second transistor including a gate coupled to the N-th gate line.

Park discloses of an array of cells formed in rows and columns, each of the cells disposed near an intersection of an N-th gate line and an M-th source line (Figure 2 shows cells 10, 12, 14 and 16 are formed at the intersection of the gate and data lines as explained in paragraph [0074].) further comprising

a first transistor including a gate coupled to the (N-2)-th gate line (Figure 2 shows that TFT4 of each cell is disposed at an N-th row and M-th column and is driven by the N-2-th gate line.), and

a second transistor including a gate coupled to the N-th gate line (Figure 2 shows that TFT3 of each cell is driven by the N-th gate line.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the transistor configuration taught by Park with the display cell structure taught by Fujiwara et al. in order to allow for an image of uniform picture quality to be displayed even when adjacent cells are not charged with a uniform voltage.

Regarding claim 10, Fujiwara et al. and Park disclose the device of claim 9.

Park also discloses the first transistor further comprising a first terminal coupled to the electrode, and a second terminal coupled to the M-th source line (Figure 2 shows that TFT4 had one terminal connect to the source line DL1 and another terminal that is connected to the pixel electrode.).

Regarding claim 11, Fujiwara et al. and Park disclose the device of claim 9.

Park also discloses the second transistor further comprising a first terminal coupled to the electrode, and a second terminal coupled to the M-th source line (Figure 2 shows that TFT3 has one terminal connected to DL1 and a second terminal connected to the pixel electrode through TFT.).

Regarding claim 23, this clam is rejected under the same rationale as claim 9.

Regarding claim 24, this clam is rejected under the same rationale as claim 9.

Regarding claim 25, this clam is rejected under the same rationale as claim 9.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

AMR A. AWAD
SUPERVISORY PATENT EXAMINER

24 September 2007